Serial No.: 09/540,591
Examiner: Hsu, Alpus

In the Abstract:

Please amend the Abstract as follows:

A bus control module as a terminal stage for a multi-stage clock/alarm distribution scheme ~~used~~ in a signaling server organized into ~~a plurality of uniquely~~ addressable shelves. ~~The signaling server includes a system timing generator, one or more clock distribution modules arranged in a nested hierarchical manner, and a plurality of bus control modules, wherein each bus control module interfaces with at least a portion of line cards disposed in a shelf.~~ ~~The~~ A system timing generator provides a framed serial control signal, SFI, addressing ~~for controlling the operation of the multi-stage clock/alarm distribution scheme. The SFI signal encodes the IDs of the~~ hierarchically arranged clock distribution modules and the bus control modules, to distribute ~~whereby~~ a system clock ~~generated by the system timing generator based on a select reference input is successively fanned out by the intermediate clock distribution modules based on address and ID information encoded in select fields of the SFI frames until the fanned out system clocks are received by~~ to the bus control modules. ~~Thereafter,~~ eEach bus control module provides a copy of the system clock to ~~the~~ line cards with which it interfaces~~controlled by it based on the SFI signal~~. The bus control module ~~also collects~~ reports ~~various~~ alarms and status signals from ~~the~~ its line interface cards ~~to be multiplexed into a framed serial signal, EAS, based on its ID, which is transmitted upstream~~ to the system timing generator using another framed serial signal. ~~for further processing and corrective action. Each line interface card provides to the bus control module a reference clock signal derived from the telecommunications network signal received thereat. A selector disposed in~~ The bus control module forwards upstream towards the system timing generator ~~selects a particular reference~~ a clock signal selected from ~~the plurality of~~ clocks signals recovered by its line interface cards from received network signals. ~~provided thereto and transports it to the next stage for transport upstream towards the system timing generator.~~